

# HIGH SPEED ELECTRICALLY PROGRAMMABLE 1024 BIT READ ONLY MEMORY

**\*50 nsec Max. Access Time**

- **Fast Access Time--50 nsec (3601-1) and 70 nsec (3601)**  
Maximum over Temperature and Supply Voltage Variation
- **Fast Programming--1 ms/Bit Typically**
- **Polycrystalline Silicon Fuse**
- **Fully Decoded--on Chip Address Decode and Buffer.**
- **Low Power Dissipation--0.5 mW/Bit Typical.**
- **DTL and TTL Compatible--Input Loading is .25 mA max.--Outputs sink 15 mA.**
- **OR-Tie Capability--Open Collector Outputs**
- **Simple Memory Expansion--2 Chip Select Input Leads.**
- **Minimum Line Reflection--Low Voltage Diode Input Clamp.**
- **Standard Packaging--16 Pin Dual In-Line Lead Configuration.**

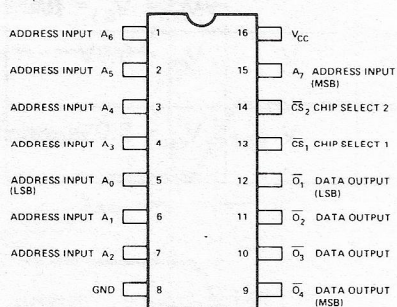
The Intel 3601/3601-1 is a 1024 bit (256 word by 4 bit) electrically programmable ROM ideally suited for uses where fast turnaround and pattern experimentation are important such as in prototypes or in small production volume systems. The PROM is manufactured with all outputs low and logic high output levels can be electrically programmed in selected bit locations. The same address inputs are used for both programming and reading.

A higher system performance is achieved by using the 3601-1. The 3601-1 gives a 25% system speed improvement over the 3601.

The 3601/3601-1 is pin compatible with the Intel metal mask 3301A ROM. The 3301A is ideal for large volume and lower cost production runs of systems initially using the PROM.

The 3601/3601-1 is manufactured with the highly reliable polycrystalline silicon fuse and the fast switching Schottky barrier diode technology.

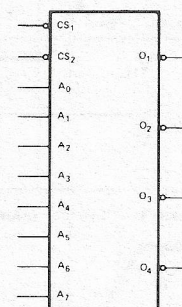
## PIN CONFIGURATION



## PIN NAMES

$A_0-A_7$	ADDRESS INPUTS
$CS_1-CS_2$	CHIP SELECT INPUTS
$O_1-O_4$	DATA OUTPUTS

## LOGIC SYMBOL





**Absolute Maximum Ratings\***

Temperature Under Bias	-65°C to +125°C
Storage Temperature	-65°C to +160°C
Output or Supply Voltages	-0.5V to 7 Volts
All Input Voltages	-1V to 5.5V
Output Currents	100mA
Programming Only:	
Output or $V_{CC}$ Voltages	10.25V
$CS_2$ Voltage	15.5V
$CS_2$ Current	100mA

**\*COMMENT**

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

**D. C. Characteristics:** All Limits Apply for  $V_{CC} = +5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+75^\circ C$ 

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. <sup>(1)</sup>	MAX.		
$I_{FA}$	ADDRESS INPUT LOAD CURRENT		-0.05	-0.25	mA	$V_{CC} = 5.25V$ , $V_A = 0.45V$
$I_{FS}$	CHIP SELECT INPUT LOAD CURRENT		-0.05	-0.25	mA	$V_{CC} = 5.25V$ , $V_S = 0.45V$
$I_{RA}$	ADDRESS INPUT LEAKAGE CURRENT			40	$\mu A$	$V_{CC} = 5.25V$ , $V_A = 5.25V$
$I_{RS}$	CHIP SELECT INPUT LEAKAGE CURRENT			40	$\mu A$	$V_{CC} = 5.25V$ , $V_S = 5.25V$
$V_{CA}$	ADDRESS INPUT CLAMP VOLTAGE		-0.7	-1.0	V	$V_{CC} = 4.75V$ , $I_A = -5.0mA$
$V_{CS}$	CHIP SELECT INPUT CLAMP VOLTAGE		-0.7	-1.0	V	$V_{CC} = 4.75V$ , $I_S = -5.0mA$
$V_{OL}$	OUTPUT LOW VOLTAGE		0.3	0.45	V	$V_{CC} = 4.75V$ , $I_{OL} = 15mA$
$I_{CEX}$	OUTPUT LEAKAGE CURRENT			100	$\mu A$	$V_{CC} = 5.25V$ , $V_{CE} = 5.25V$
$I_{CC}$	POWER SUPPLY CURRENT		90	130	mA	$V_{CC} = 5.25V$ , $V_{A0} \rightarrow V_{A7} = 0V$ , $V_{S0} = V_{S1} = 0V$
$V_{IL}$	INPUT "LOW" VOLTAGE			0.85	V	$V_{CC} = 5.0V$
$V_{IH}$	INPUT "HIGH" VOLTAGE	2.0			V	$V_{CC} = 5.0V$

Note 1: Typical values are at 25°C and at nominal voltage.



**A. C. Characteristics**  $V_{CC} = +5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+75^\circ C$ 

SYMBOL	PARAMETER	MAXIMUM LIMITS			UNIT	CONDITIONS
		0°C	25°C	75°C		
$t_{A++}, t_{A--}$ $t_{A+-}, t_{A-+}$	Address to Output Delay (3601)	70	60	70	ns	Both C.S. lines must be at ground potential to activate the PROM.
$t_{A++}, t_{A--}$ $t_{A+-}, t_{A-+}$	Address to Output Delay (3601-1)	50	50	50	ns	
$t_{S++}, t_{S--}$	Chip Select to Output Delay	25	25	25	ns	

**Capacitance** <sup>(1)</sup>  $T_A = 25^\circ C$ 

SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
$C_{INA}$	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
$C_{INS}$	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
$C_{OUT}$	Output Capacitance	7	12	pF	$V_{CC} = 5V$ $V_{OUT} = 2.5V$

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

**Switching Characteristics****Conditions of Test:**

Input pulse amplitudes - 2.5V

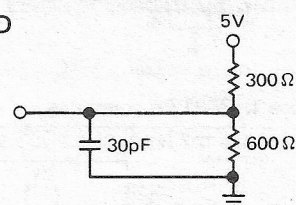
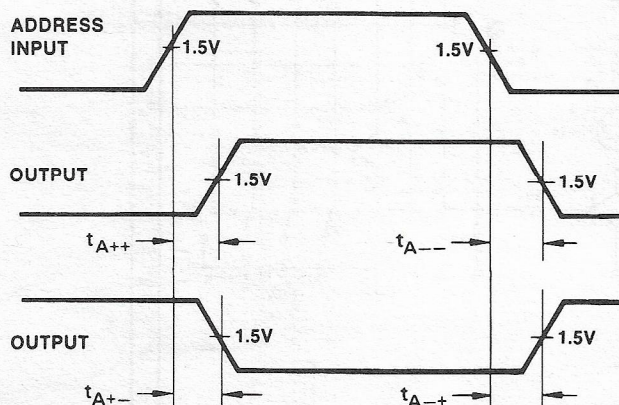
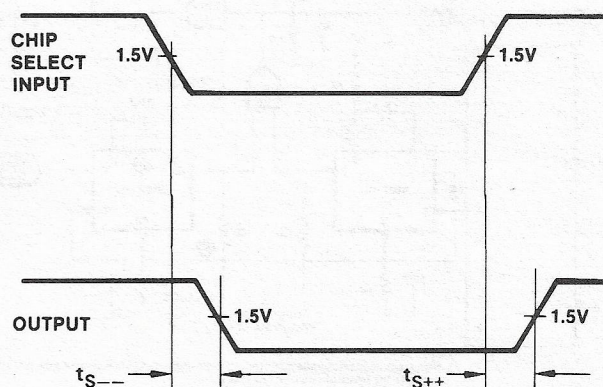
Input pulse rise and fall times of

5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

Output loading is 15 mA and 30 pF

Frequency of test - 2.5 MHz

**15 mA TEST LOAD****Waveforms****ADDRESS TO OUTPUT DELAY****CHIP SELECT TO OUTPUT DELAY**



### Manually Programming the 3601 (or 3601-1)

The 3601 may be programmed using the basic circuit of Figure 1. Address inputs are at standard TTL levels. Only one output may be programmed at a time. The output to be programmed must be connected to  $V_{CC}$  through a  $300\Omega$  resistor. This will force the proper programming current (3-6mA) into the output when the  $V_{CC}$  supply is later raised to 10V. All other outputs must be held at a TTL low level (0.4V).

The programming pulse generator produces a series of pulses to the 3601  $V_{CC}$  and  $CS_2$  leads.  $V_{CC}$  is pulsed from a low of  $4.5 \pm .25V$  to a high of  $10 \pm .25V$ , while  $CS_2$  is pulsed from a low of ground (TTL logic 0) to a high of  $15 \pm 0.5V$ . It is important to accurately maintain these voltage levels, otherwise, improper programming may result. The pulses applied must maintain a duty cycle of  $50 \pm 10\%$  and start with an initial width of  $1 (\pm 10\%)\mu s$ , and increase linearly over a period of approximately 100ms to a maximum width of  $8 (\pm 10\%)\mu s$ . Typical devices have their fuse blown within 1ms, but occasionally a fuse may take up to 400ms. During the application of the program pulse, current to  $CS_2$  must be limited to 100mA. The output of the 3601 is sensed when  $CS_2$  is at a TTL low level output. A programmed bit will have a TTL high output. After a fuse is blown, the  $V_{CC}$  and  $CS_2$  pulse trains must be applied for another  $100\mu s$ . One circuit which can be used to generate this pulse train is shown in Figure 2, while the characteristics of the pulse train are shown in Figure 3.

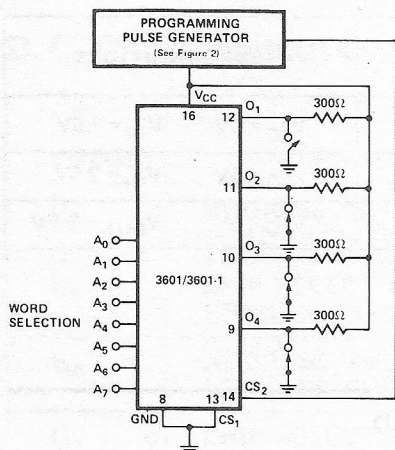


Figure 1. 3601 Programming

a.  $V_{CC}$  (pin 16)

b.  $CS_2$  (pin 14)

c. Sensed Output Waveform

d. Programming Pulse Width ( $V_{CC}$  and  $CS_2$ ) versus Programming Time

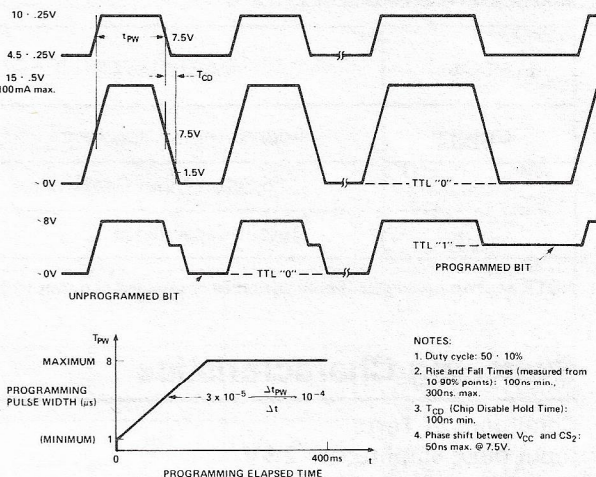
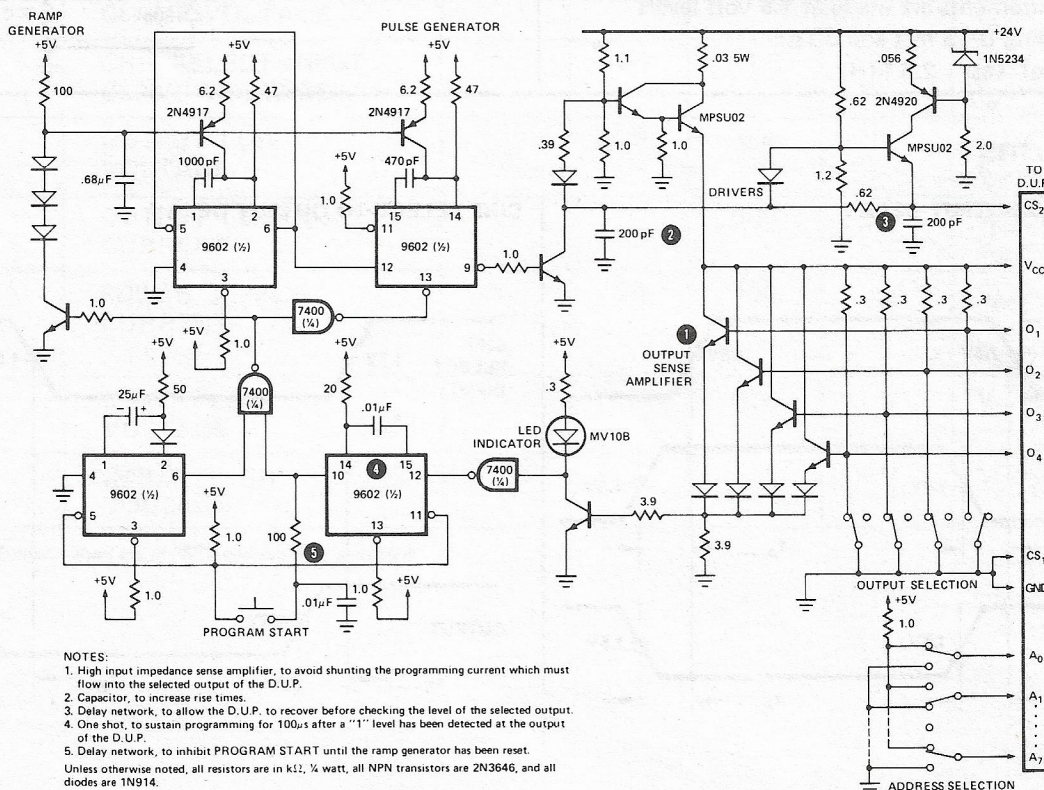


Figure 3. Pulses During Programming



- NOTES:
1. High input impedance sense amplifier, to avoid shunting the programming current which must flow into the selected output of the D.U.P.
  2. Capacitor, to increase rise times.
  3. Delay network, to allow the D.U.P. to recover before checking the level of the selected output.
  4. One shot, to sustain programming for  $100\mu s$  after a "1" level has been detected at the output of the D.U.P.
  5. Delay network, to inhibit PROGRAM START until the ramp generator has been reset.
- Unless otherwise noted, all resistors are in k $\Omega$ ,  $\frac{1}{2}$  watt, all NPN transistors are 2N3646, and all diodes are 1N914.

Figure 2. 3601 Programmer